42/50G2 PDP modules vertical line issue repair method

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I. TV models using G2 PDP panels.

There are reported two kind of vertical noise in the field related to PDP panels 42G2 and 50G2 series caused by control board assembly.

- 1.- Vertical line with same interval.
- 2.- Vertical line without same interval.

This bulletin shows analysis and repair method for both kind of issues.

TV MODELS USING 42G2 SERIES PANELS

| IV MODELS USING 42G2 SERIES PANELS. | | | | | |
|-------------------------------------|--------------------|----|--------------------|--|--|
| No | Model Name | No | Model Name | | |
| 1 | 42PQ20-UA.ACCLLHR | 27 | 42PQ20-UA.ACCALHR | | |
| 2 | 42PQ20-UA.ACCLLJR | 28 | 42PQ20-UA.AUSALHR | | |
| 3 | 42PQ20-UA.AUSLLHR | 29 | 42PQ20-UA.AWMALHR | | |
| 4 | 42PQ20-UA.AUSLLJR | 30 | 42PQ30-UA.ACCALHR | | |
| 5 | 42PQ20-UA.AWMLLHR | 31 | 42PQ30-UA.AUSALHR | | |
| 6 | 42PQ20-UA.AWMLLJR | 32 | 42PQ30-UD.AWMALHR | | |
| 7 | 42PQ30-UA.ACCLLHR | 33 | 42PQ30C-UA.AUSALHR | | |
| 8 | 42PQ30-UA.ACCLLJR | 34 | 42PQ30R-MA.AWCALJR | | |
| 9 | 42PQ30-UA.AUSLLHR | 35 | 42PQ30R-MA.AWFALJR | | |
| 10 | 42PQ30-UA.AUSLLJR | 36 | 42PQ30R-MA.AWHALJR | | |
| 11 | 42PQ30-UD.AWMLLHR | 37 | 42PQ30R-MA.AWPALJR | | |
| 12 | 42PQ30-UD.AWMLLJR | 38 | 42PQ60-UA.ACCALHR | | |
| 13 | 42PQ30C-UA.AUSLLHR | 39 | 42PQ60-UA.AWMALHR | | |
| 14 | 42PQ30R-MA.AWCLLJR | 40 | 42PQ60R-MA.AWCALJR | | |
| 15 | 42PQ30R-MA.AWFLLJR | 41 | 42PQ60R-MA.AWFALJR | | |
| 16 | 42PQ30R-MA.AWHLLJR | 42 | 42PQ60R-MA.AWHALJR | | |
| 17 | 42PQ30R-MA.AWPLLJR | 43 | 42PQ60R-MA.AWPALJR | | |
| 18 | 42PQ31-UD.AWMLLHR | | | | |
| 19 | 42PQ60-UA.ACCLLHR | | | | |
| 20 | 42PQ60-UA.ACCLLJR | | | | |
| 21 | 42PQ60-UA.AWMLLHR | | | | |
| 22 | 42PQ60-UA.AWMLLJR | | | | |
| 23 | 42PQ60R-MA.AWCLLJR | | | | |
| 24 | 42PQ60R-MA.AWFLLJR | | | | |
| 25 | 42PQ60R-MA.AWHLLJR | | | | |
| 26 | 42PQ60R-MA.AWPLLJR | | | | |

TV MODELS USING 50G2 SERIES PANELS.

| No | Model Name | No | Model Name |
|----|--------------------|----|--------------------|
| 1 | 50PQ20-UA.ACCLLHR | 27 | 50PQ20-UA.ACCALHR |
| 2 | 50PQ20-UA.ACCLLJR | 28 | 50PQ20-UA.AUSALHR |
| 3 | 50PQ20-UA.AUSLLHR | 29 | 50PQ20-UA.AWMALHR |
| 4 | 50PQ20-UA.AUSLLJR | 30 | 50PQ30-UA.ACCALHR |
| 5 | 50PQ20-UA.AWMLLHR | 31 | 50PQ30-UA.AUSALHR |
| 6 | 50PQ20-UA.AWMLLJR | 32 | 50PQ30-UD.AWMALHR |
| 7 | 50PQ30-UA.ACCLLHR | 33 | 50PQ30C-UA.AUSALHR |
| 8 | 50PQ30-UA.ACCLLJR | 34 | 50PQ30R-MA.AWCALJR |
| 9 | 50PQ30-UA.AUSLLHR | 35 | 50PQ30R-MA.AWFALJR |
| 10 | 50PQ30-UA.AUSLLJR | 36 | 50PQ30R-MA.AWHALJR |
| 11 | 50PQ30-UD.AWMLLHR | 37 | 50PQ30R-MA.AWPALJR |
| 12 | 50PQ30-UD.AWMLLJR | 38 | 50PQ60-UA.ACCALHR |
| 13 | 50PQ30C-UA.AUSLLHR | 39 | 50PQ60-UA.AWMALHR |
| 14 | 50PQ30R-MA.AWCLLJR | 40 | 50PQ60R-MA.AWCALJR |
| 15 | 50PQ30R-MA.AWFLLJR | 41 | 50PQ60R-MA.AWFALJR |
| 16 | 50PQ30R-MA.AWHLLJR | 42 | 50PQ60R-MA.AWHALJR |
| 17 | 50PQ30R-MA.AWPLLJR | 43 | 50PQ60R-MA.AWPALJR |
| 18 | 50PQ31-UD.AWMLLHR | | |
| 19 | 50PQ60-UA.ACCLLHR | | |
| 20 | 50PQ60-UA.ACCLLJR | | |
| 21 | 50PQ60-UA.AWMLLHR | | |
| 22 | 50PQ60-UA.AWMLLJR | | |
| 23 | 50PQ60R-MA.AWCLLJR | | |
| 24 | 50PQ60R-MA.AWFLLJR | | |
| 25 | 50PQ60R-MA.AWHLLJR | | |
| 26 | 50PQ60R-MA.AWPLLJR | | |

II. PDP module (G2 models) Vertical Noise type

✓ There are two types of Picture (Vertical) noise upon DDR Memory for 42/50G2 PDP module.

1. Vertical <u>line</u> with same interval (16pixels)



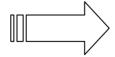
2. Vertical <u>line</u> without same interval (8pixels, 16pixels or 32pixels)





II. PDP module (G2 models) Vertical Noise type

Vertical line with same interval (16pixels)





CHECK PROCEDURE:

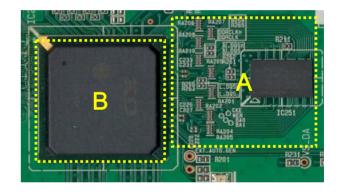
This problem is mostly related to failure in DQ signal paths from DDR2 memory IC251 to BGA IC201.

- A. Check the components solder quality, foils and via holes integrity.
- B. Press BGA IC firmly to check for bad solder.

Refer to A1 figure in page 5.



Check points

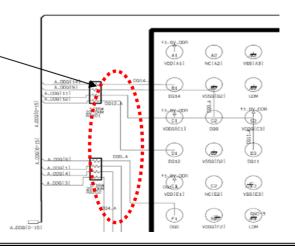


C. Check diode value of the16 DQ lines using multi-meter,

<u>GND(+)-to-DQ line(-)</u> (refer to A3 picture in the last slide)

Normal diode voltage drop is (0.4 to 0.5 Vdc).

If everything is OK and failure persist, change the control board assy.



II. PDP module (G2 models) Vertical Noise type

2. Vertical line without same interval (8pixels, 16pixels or 32pixels).



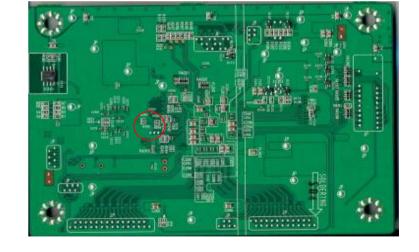


CHECK PROCEDURE:

- Check the control board DQS Resistors coming out from DDR memory to BGA IC (backside R282, R283, R284, R285)
 - DQS (local clock function) resistor value must be 470Ω .

If 1K Ω resistor value is found, change to 470 Ω (1k $\Omega \rightarrow$ 470 Ω).

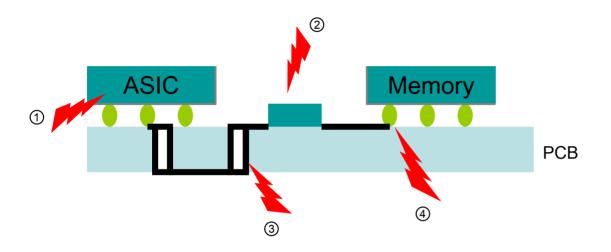
- $1k\Omega$ has some potential probability to cause vertical lane when repeatedly connected and disconnect of LVDS cable.
- B. Check diode value of the 4 DQS lines.
 (refer to A3 picture in the last slide).
 Normal diode voltage drop is (0.4 to 0.5 Vdc).



If everything is OK and failure persist, change the control board assy.

A1. Vertical Noise Failure cause

Possible Failure Cause of Picture (Vertical) Noise upon DDR Memory



- **※** Failure cause:
- ① Pin fail: Diode check with multi-meter.
- ② Resistor Crack and soldering problem : visual inspection
- ③ Via hole crack: Diode check, resistor check visually and using multi-meter.
- Ball crack and soldering problem in BGA IC's: Press devices toward PCB

A3. Measuring Diode value of DQ and DQS

✓ Diode check using Multi-meter

